check generator comprises the step of precharging the cyclical redundancy check generator to a second logic level.

13. (New) The method of claim 8, wherein an check word buffer is connected to the cyclical redundancy check generator and the step of performing the cyclical redundancy check comprises the steps of:

activating the cyclical redundancy check generator when the cyclical redundancy check strobe is detected;

generating an error check word from the data latched in the data latch; and

comparing the error check word with data in the check word buffer.

14. (New) A method for cyclical redundancy check error generation in a system having a cyclical redundancy check generator, a data latch, and two data buffers connected by a plurality of data bus lines, the data latch having a precharge circuit, and the data sources having data outputs, the method comprising the steps of:

inhibiting the cyclical redundancy check generator and the data outputs;

precharging the plurality of data bus lines to a first logic level until a cyclical redundancy check strobe is detected;

turning off the precharge circuit;

activating the data outputs from one of the data buffers to modulate charge on the plurality of data bus lines;

waiting for a sufficient time for the plurality of data bus lines to develop a charge differential;

latching data on the plurality of data bus lines in the data latch; and

performing a cyclical redundancy check on the data latched in the data latch.

15. (New) A programmable error detection and correction system comprising:

an error check module programmable for generating and comparing error check words;

a first parallel data bus programmable for transferring data from an edit buffer to a first data port;

a second parallel data bus programmable for transferring data from the first data port to the error check module and to the edit buffer, and further programmable for transferring data from the edit buffer to the error check module;

a third parallel data bus programmable for transferring an error check word between the error check module and the edit buffer;

a control module for programming the first, second and third data buses, and the error check module to operate according to a plurality of error processing modes.

16. (New) The programmable error detection and correction system of claim 15, wherein a first error processing mode causes the control module to program the second data bus to transfer data from the edit buffer to the error check module, causes the control module to program the third data bus to transfer a first error check word from the edit buffer to the error check module, and causes the error check module to generate a second error check word based on the data and to compare the first and second error check words.

17. (New) The programmable error detection and correction system of claim 15, wherein a second error processing mode causes the control module to program the second data bus to transfer data from the first data port to the edit buffer and to the error check module, causes the control module to program the error check module to generate an error check word from the data, and causes the control module to program the third data bus to transfer the error check word to the edit buffer.

18. (New) The programmable error detection and correction system of claim 15, wherein a third error processing mode causes the control module to program the first data bus to transfer first data from the edit buffer to the first data port, and causes the control module to program the second data bus to transfer second data from the first data port to the edit buffer.

19. (New) The programmable error detection and correction system of claim 18, wherein the edit buffer comprises two data portions and the control module programs the first and second buses to transfer data to and from the data portions according to a plurality of data protocols.

20. (New) The programmable error detection and correction system of claim 19, wherein a first data protocol stores a header word in one of the data portions and raw data in the other data portion.

21. (New) The programmable error detection and correction system of claim 19, wherein a second data protocol stores header data in one of the data portions and prepend and postpend data in the other data portion.

22. (New) The programmable error detection and correction system of claim 19, wherein a third data protocol stores raw data in both data portions.

23. (New) The programmable error detection and correction system of claim 18, wherein the error check module generates and compares cyclical redundancy check words.

24. (New) The programmable error detection and correction system of claim 15, wherein the control module programs a fourth parallel data bus to transfer data between a second data port and the edit buffer.

Respectfully submitted,

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